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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/103,873	06/24/1998	YOSHIHISA NAGANO	YAO-3950	3577

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ANDREW L NEY
RATNER & PRESTIA
SUITE 301 ONE WESTLAKES BERWYN
P O BOX 980
VALLEY FORGE, PA 194820980

EXAMINER
DIAZ, JOSE R

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

15

Office Action Summary	Application No.	Applicant(s)	
	09/103,873	NAGANO ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 29-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 29-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *09 January 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

➢ Claims 1-10 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Specification in view of Matsuura et al. (US Patent No. 5,132,774).

Regarding claims 1 and 29, Applicant acknowledges that is well known in the art to form an integrated circuit (4) on a supporting substrate (1); a capacitor (10) having a lower electrode (7), a dielectric film (8), and an upper electrode (9); a first interlayer insulating film (11) provided so as to directly cover the capacitor; a first interconnect (14) electrically connected to the integrated circuit (4) and the capacitor (10) through a first

contact hole (12) formed in the first interlayer insulating film (11); a second interlayer insulating film (15) provided so as to directly cover the first interconnect (14) and the first interlayer insulating film (11); a second interconnect (17) electrically connected to the first interconnect (14) through a second contact hole (16) formed in the second interlayer insulating film (15); and a passivation layer (18) provided so as to cover the second interconnect (17) (See figures 10A-10E). However, Applicant's states that Figures 10A-10E fail to teach a second interlayer insulating film having a tensile stress. Matsuura et al. teach that is well known in the art to provide a second interlayer insulating film (14, 35) having a tensile stress directly over a first interconnect (12, 32, 34) and a first interlayer insulating film (20, 33) (see Figs. 1E and 6A-6B). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Applicant's Specification to include a second interlayer insulating film having a tensile stress directly over a first interconnect and a first interlayer insulating film. The ordinary artisan would have been motivated to modify Applicant's Specification in the manner described above for at least the purpose of providing a smooth upper surface so that a second interconnect pattern is easily formed without disconnection on the interlayer insulating film.

Regarding claim 2, Applicant acknowledges that the dielectric film (8) is formed of either a dielectric material having a high dielectric constant or ferroelectric material (Page 2, lines 26-28).

Regarding claim 3, the Applicant's Specification, as stated supra, essentially discloses a well known semiconductor device but fails to disclose a second interconnect

on the second interlayer insulating film provided so as to cover at least a part of the capacitor. Matsuura et al. teach that is well known in the art to form a second interconnect (36) over at least a part of the capacitor (27, 28, 29) (see Figs. 6A-6B). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Applicant's Specification to include a second interconnect on the second interlayer insulating film provided so as to cover at least a part of the capacitor. The ordinary artisan would have been motivated to modify Applicant's Specification in the manner described above for at least the purpose of electrically connecting the first wiring layer.

Regarding claim 4, Applicant's Specification, as stated supra, essentially discloses a well-known semiconductor device but fails to disclose a passivation layer that is formed from a laminate including a silicon oxide film and a silicon nitride film. Matsuura et al. teach that is well known in the art to form a passivation layer (37) of a laminate including silicon oxide and silicon nitride films (see col. 7, lines 59-62). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Applicant's Specification to include a passivation layer that is formed from a laminate including a silicon oxide film and a silicon nitride film. The ordinary artisan would have been motivated to modify Applicant's Specification in the manner described above for at least the purpose of passivating and protecting the exposed wiring layers.

Regarding claim 5, Applicant's Specification, as stated supra, essentially discloses a well-known semiconductor device but fails to show a hydrogen-supplying

layer. Matsuura et al. teach that is well known in the art to provide a hydrogen-supplying layer (i.e. silicon nitride) (13, 16) (see Figures 1E and 5A-5B). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Applicant's Specification to include a hydrogen supplying layer between the first interconnect and the second interlayer insulating film. The ordinary artisan would have been motivated to modify Applicant's Specification in the manner described above for at least the purpose of reducing the stress of the interlayer insulating film (see col. 7, lines 3-6 and 7-10)

Regarding claims 6 and 10, Applicant's Specification, as stated supra, essentially discloses a well-known semiconductor device but fails to disclose that the first and second interconnect layers are formed from a laminate including aluminum and titanium nitride. Matsuura et al. teach that it is well known in the art to form first and second interconnect layers of a laminate including aluminum and titanium nitride (see col. 7, lines 47-59). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Applicant's Specification to include first and second interconnect layers formed of a laminate including aluminum and titanium nitride. The ordinary artisan would have been motivated to modify Applicant's Specification in the manner described above for at least the purpose of providing electrical interconnection in the device.

Regarding claim 7, Applicant's Specification, as stated supra, essentially discloses a well-known semiconductor device but fails to disclose a Si-OH bond absorption coefficient of the insulating film at a wavelength corresponding to 3450 cm^{-1}

of 800 cm^{-1} or less. Matsuura et al. teach that the Si-OH bond absorption coefficient of the second insulating film at a wavelength corresponding to 3450 cm^{-1} is 800 cm^{-1} or less (see Figs 3B). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Applicant's Specification to include a Si-OH bond absorption coefficient of the second insulating film at a wavelength corresponding to 3450 cm^{-1} of 800 cm^{-1} or less. The ordinary artisan would have been motivated to modify Applicant's Specification in the manner described above for at least the purpose of providing a smooth upper surface so that a second interconnect pattern is easily formed without disconnection on the interlayer insulating film.

Regarding claim 8, Official Notice is taken with respect to the limitation regarding a second interlayer insulating film having a tensile stress of 1×10^7 to 3×10^9 dyn/cm^2 since one of ordinary skill in the art would recognize that APCVD layers such as the a second interlayer insulating film (14, 35) of Matsuura et al. has a tensile stress of about 3×10^9 $dynes/cm^2$ (see for example Table 2 of Wolf et al. ("Silicon Processing for the VLSI Era Volume 1: Process Technology", Lattice Press, 1986, pp. 182-194).

Regarding claim 9, Applicant's Specification, as stated supra, essentially discloses a well-known semiconductor device but fails to disclose a second interlayer insulating film having a thickness of 0.3 μm to 1 μm. Matsuura et al. teach that it is well known in the art to provide an interlayer insulating film having a thickness of about 1 μm (column 5, lines 24-32). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Applicant's

Specification to include a an interlayer insulating film having a thickness of about 1 μm. The ordinary artisan would have been motivated to modify Applicant's Specification in the manner described above for at least the purpose of providing a smooth upper surface so that a second interconnect pattern is easily formed without disconnection on the interlayer insulating film.

Regarding claims 30-31, Applicant's Specification in view of Matsuura et al. teach the claimed invention except for an optimum remnant polarization of about 10 $\mu C/cm^2$. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide a dielectric film having a remnant polarization of 10 $\mu C/cm^2$, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

➢ Applicant's arguments with respect to claims 1-10 and 29-31 have been considered but are moot in view of the new ground(s) of rejection.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00 - 5:00 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
April 7, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800